AMENDMENTS TO THE CLAIMS

(1-18) Canceled

19 (New).   A method of verifying a processor design against a processor specification, the method comprising:

    a)   creating a verification environment;

    b) executing an instruction sequence in a first simulation process within the verification environment, the first simulation process comprising the execution of the instruction sequence according to a representation of the processor specification;

    c)   executing the instruction sequence in a second simulation process, the second simulation process comprising the execution of the instruction sequence according to a representation of the processor design; and

    d) comparing results of the first simulation process with results of the second simulation process within the verification environment in order to verify the processor design,

wherein the representation of the processor specification is a machine-executable representation and the method further comprises processing the processor specification with a compiler to generate the machine-executable representation of the processor specification for the first simulation process.

20 (New).   A method according to claim 19, wherein the processor specification comprises one or more verifiable elements.

21 (New).   A method according to claim 20 wherein the verification environment maintains a current state of the one or more verifiable elements.

22 (New).   A method according to claim 19, wherein the processor specification further comprises at least one description of one or more instructions to be executed by the processor.

23 (New).   A method according to claim 22, wherein each said at least one instruction description comprises zero or more actions associated with the instruction.

24 (New).   A method according to claim 19, wherein the processor specification further comprises a description of a stimulus which may cause an exception condition in the processor.

25 (New).   A method according to claim 24, wherein said stimulus description comprises zero or more actions associated with the stimulus.

26 (New).   A method according to claim 25, further comprising executing actions associated with a stimulus, wherein zero or more entries are added to a specification queue.

27 (New).   A method according to claim 20, wherein each of the verifiable elements is associated with a respective specification queue, the method further comprising:

executing actions associated with one or more instructions from the instruction sequence within the first simulation, wherein zero or more entries are added to the specification queue.

28 (New).   A method according to claim 27, further comprising executing actions associated with a stimulus, wherein zero or more entries are added to a specification queue.

29 (New).   A method according to claim 20, wherein each of the verifiable elements is associated with a respective design queue.

30 (New).   A method according to claim 19, wherein the verification environment receives one or more notifications from the second simulation, the one or more notifications being generated by the operation of the second simulation.

31 (New).   A method according to claim 30 further comprising:

the verification environment analysing the one or more received notifications; and

the verification environment generating one or more entries in one or more design queues in response to the received notifications.

32 (New).   A method according to claim 31, wherein the processor specification comprises one or more verifiable elements and each of the verifiable elements is associated with a respective specification queue, the method further comprising:

executing actions associated with one or more instructions from the instruction sequence within the first simulation, wherein zero or more entries are added to the specification queue; and

the verification environment verifying each verifiable element for which the design queue or the specification queue comprise one or more entries, by comparing the respective queues.

33 (New). A method according to claim 32, wherein the verification environment:

identifies reconcilable entries within each queue; and

removes the reconcilable entries from the design queue and the specification queue and updates the state of the corresponding verifiable elements.

34 (New).   A method according to claim 32 wherein the verification environment reports an error if the design queue can not be reconciled with the compared specification queue.

35 (New).   A method according to claim 19, wherein the verification environment analyses the processor specification to determine a plurality of processor memory elements.

36 (New).   A method according to claim 35, wherein the verification environment further provides memory resources to the second simulation to implement the plurality of processor memory elements.

37 (New).   A computer-readable medium comprising code which, when executed causesa method according to claim 19 to be performed.